REMARKS/ARGUMENTS

Claims 1-25 are pending. Claim 11 has been amended to correct a typographical error by making the second instance of "architecture" plural so that the claim reads "a first architecture of a plurality of fixed architectures".

35 U.S.C. §101, Nonpatentable Subject Matter

Claims 21-25 stand rejected under 35 USC 101 because it is directed to non-statutory subject matter. The Examiner asserts that the claim is directed to software, and it is non-patentable since there is no hardware structure claimed on which the software can be executed. This rejection is respectfully traversed and reconsideration is respectfully requested.

"A claim is limited to a practical application when the method, as claimed, produces a concrete, tangible and useful result; i.e., the method recites a step or act of producing something that is concrete, tangible and useful. See AT&T, 172 F.3d at 1358, 50 USPQ2d at 1452." MPEP Manual of Patent Examining Procedures § 2106. It is respectfully submitted that the claimed method in claims 21-25 produces the concrete, tangible, and useful result of allocating hardware resources within an adaptive integrated circuit more efficiently. In AT&T, the Federal Circuit held patentable a claim for

> [a] method for use in a telecommunications system in which interexchange calls initiated by each subscriber are automatically routed over the facilities of a particular one of a plurality of interexchange carriers associated with that subscriber, said method comprising the steps of:
> generating a message record for an interexchange call between an originating subscriber and a terminating subscriber, and
> including, in said message record, a primary interexchange carrier (PIC) indicator having a value which is a function of whether or not the interexchange carrier associated with said terminating subscriber is a predetermined one of said interexchange carriers.

The message records are stored in electronic format, which are transmitted from one computer system to another and reformatted to ease processing of the information. Id. at 1354. This claim is generally directed to a method for processing electronic data on a computer system. Note that this claim does not mention any specific computer hardware on which the

method is to be implemented or that it is a computer-implemented method. Thus, a specific mention of hardware on which a method might be implemented is not required. Similarly, claims 21-25 are directed toward a method for an adaptive computer integrated circuit (like the computer system of AT&T) that processes configuration information. Due to the allowance of the similarly situated AT&T claim, it is respectfully submitted that claims 21-25 are directed to patentable subject matter.

35 U.S.C. §102 Rejection, New

Claims 21 and 23-25 stand rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 6,046,603 to New. This rejection is respectfully traversed and reconsideration is respectfully requested.

New fails to anticipate claim 21 because New fails to disclose or suggest every element of claim 21. For example, claim 21 recites "*configuring a first group of heterogeneous computational elements*". In the Office Action, the Examiner asserts that New's configurable logic blocks (CLB), corresponding to elements 9-16 of Fig. 1, and the accompanying discussion at column 5 lines 39-46 anticipate configuring a first group of heterogeneous computational elements.

Fig. 1 of New shows an array of CLBs numbered 1-24. The CLBs are homogeneous in that each CLB has the same physical structure. Additionally, at column 5, lines 39-46, New does not discuss the CLBs differing from each other. It is also standard practice in the field of programmable gate arrays (FPGA) that FPGAs are made of identical logic arrays. New (6,046,603) or patent number 6,046,603 does not discuss the CLBs differing in physical structure. In the specification at paragraph 35, the term "heterogeneous" is used to describe matrices 150 that differ from each other, and the term "heterogeneous" is used to describe computational elements 250 on page 11, line 20-21. Because the CLBs in New are not heterogeneous, New does not disclose or suggest configuring a first group of heterogeneous computational elements. For at least this reason, it is respectfully submitted that New does not anticipate claim 21.

Claims 22-25 are dependent on claim 21, and thus derive patentability therefrom for at least the reasons claim 21 is allowable.

35 U.S.C. §103 Rejection, New in view of Wirthlin et al.

Claims 1-20 and 22 stand rejected under 35 USC 103(a) as being unpatentable over New (6,046,603) in view of Wirthlin et al. (Wirthlin). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claims 1-5

Claim 1 is allowable over the cited references, alone or in combination, as those references fail to disclose or suggest all the elements of claim 1. For example, claim 1 recites "*a plurality of heterogeneous computational elements, ... wherein a first group of heterogeneous computational elements is configurable to form a first functional unit to implement a first function*". In the Office Action, the Examiner asserts that the "AND" gates 1A-24A and the associated reconfiguration circuits 1B-24B being inside each one of a group (9-16 of Fig. 1) of New's CLBs describe a group of heterogeneous computational elements configurable to form a first functional unit to implement a first function.

As mentioned above, the fact that a CLB has more than one component does not make it part of a heterogeneous group since the term heterogeneous refers to the relation of the CLBs to each other. Since the CLBs in New do not differ from each other, they are not heterogeneous computational elements. In section 2.2 and elsewhere, Wirthlin discusses FPGAs generically and does not mention the physical structure of the logical arrays. Since it is industry practice for an FPGA to have identical logic arrays, the FPGAs in Wirthlin also do not describe heterogeneous computational elements. For at least this reason, it is respectfully submitted that New and Wirthlin do not teach, disclose or even suggest claim 1.

Claims 2-5 are dependent on claim 1, and thus derive patentability therefrom for at least the reasons claim 1 is allowable.

Claims 6-10

Claim 6 is allowable over the cited references, alone or in combination, as those references fail to disclose or suggest all the elements of claim 6. For example, claim 6 recites "*a*

plurality of heterogeneous computational units, each heterogeneous computational unit having a plurality of fixed computational elements". In the Office Action, the Examiner asserts that New's CLBs (column 1, lines 56-60 and column 5, lines 39-46) correspond to heterogeneous computational units and that elements 1A-24A and 1B-24B of Fig. 1 correspond to the fixed computational elements.

As mentioned above, each CLB in New has the same two identical components, for example 1A and 1B of CLB 1 in FIG. 1. Thus, the CLBs are identical and are not heterogeneous when compared to each other. As mentioned above, the FPGAs in Wirthlin also do not have heterogeneous computational units. For at least this reason, it is respectfully submitted that New and Wirthlin do not teach, disclose or even suggest claim 6.

Claims 7-10 are dependent on claim 6, and thus derive patentability therefrom for at least the reasons claim 6 is allowable.

Claims 11-15

Claim 11 is allowable over the cited references, alone or in combination, as those references fail to disclose or suggest all the elements of claim 11. For example, claim 11 recites "*a plurality of heterogeneous computational elements, the plurality of heterogeneous computational elements including a first computational element and a second computational element*". In the Office Action, the Examiner either asserts that New's elements 1A-24A and 1B-24B correspond to both the heterogeneous computational elements as well as the first and second computational elements included within the heterogeneous computational elements, or the Examiner asserts that New's CLBs correspond to the heterogeneous computational elements and elements 1A-24A and 1B-24B correspond to the first and second computational elements.

New's elements 1A-24A and 1B-24B cannot correspond to both the heterogeneous computational elements and the first and second computational elements included within them. That is to say, an element cannot be both the container and the objects included within it. Additionally, New's CLBs cannot correspond to the heterogeneous computational elements because the CLBs in New are not heterogeneous. The FPGAs in Wirthlin also do not have heterogeneous computational elements. For at least this reason, it is respectfully submitted that New and Wirthlin do not teach, disclose or even suggest claim 11.

Claims 12-15 are dependent on claim 11, and thus derive patentability therefrom for at least the reasons claim 11 is allowable.

Claims 16-20

Claim 16 is allowable over the cited references, alone or in combination, as those references fail to disclose or suggest all the elements of claim 16. For example, claim 16 recites "*a plurality of heterogeneous computational elements, the plurality of heterogeneous computational elements including a first computational element and a second computational element*". As this claim limitation also appears in claim 11, claim 16 is allowable for at the same reasons as claim 11.

Claims 17-20 are dependent on claim 16, and thus derive patentability therefrom for at least the reasons claim 16 is allowable.

Claim 22

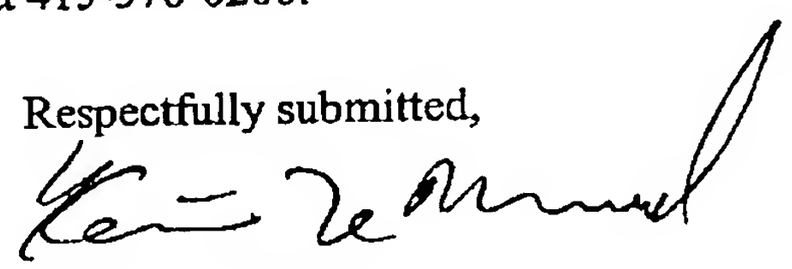
Claim 22 is dependent on claim 21, and thus derives patentability therefrom for at least the reasons claim 21 is allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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